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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,272	07/24/2003	Chien-Chih Chen	56410-DIV (71987)	9571

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EDWARDS & ANGELL, LLP
P.O. BOX 55874
BOSTON, MA 02205

EXAMINER	
ROMAN, ANGEL	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,272	CHEN ET AL.	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-18 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-18 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 13-18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. U.S. Patent 6,566,741 B2 in view of Wada et al. U.S. Patent 6,602,734 B1.

Lin discloses a method of fabricating a semiconductor package comprising; preparing a chip carrier (16, 80, 112) having a first side, and a second side opposing the first side and finally removed from an engaged surface of a mold in a die molding process (see figure 1), wherein at least one grounding means (61, 62, 63, 98) is formed on the second side corresponding in position to en eject pin (32, 102, 122) of the mold (see figure 3); performing a die bonding process for mounting at least one semiconductor chip (18, 84, 110) on the first side of the chip carrier (16, 80, 102); providing a plurality of conducting elements for electrically connecting the semiconductor chip (18, 84, 110) to the carrier (16, 80, 102) (see figure 3); performing a molding process for forming an encapsulant (13, 130) for encapsulating the semiconductor chip (18, 84 110) and the conductive elements on the first side of the carrier (see figures 1 and 4D); performing a de-molding process for ejecting the semiconductor package from the mold by using eject pins on the mold; and performing a ball implanting process for implanting a plurality of solder balls 86 on the second side

of the chip carrier (see figure 3). Lin et al. also discloses the chip carrier comprising; a base layer having a first surface and a second surface opposing the first surface; a plurality of conductive traces (90) disposed on the first surface of the base layer and electrically connected to the semiconductor chip (see figure 3); a plurality of ball pads formed on the second surface of the base layer for implanting the solder balls 86 thereon; a plurality of vias for electrically connecting the conductive traces to the ball pads respectively (see figure 3); a die pad formed on the first surface of the base layer for mounting the semiconductor chip thereon; and a solder mask layer 28 deposited on each of the first an second surfaces of the base layer in a manner that part of the conductive traces electrically connected to the semiconductor chip on the first surface and the ball pads on the second surface are respectively exposed to outside of the solder mask layer (see column 3, lines 13-20). The grounding means are fabricated form gold and are exposed trough the solder mask layer and are electrically connected to a grounding trace disposed on the first side of the chip carrier by a grounding via formed through the base layer, the grounding means corresponding in position to eject pins of the mold (see figure 3).

Lin et al. is applied as above but lacks anticipation on disclosing a singulating process for forming individual packages and disclosing a plating process for forming the grounding means. Wada et al. discloses a process for forming individual packages by singulating encapsulated semiconductor devices formed on a carrier (see figure 14) and a plating gold on pads (see column 5, lines 19-22); therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made

to disclose a singulating process as disclosed in Wada et al. in the primary reference of Lin et al. since Lin et al. already suggest using a strip of several packages and separating the packages is conventionally performed to obtained individual devices. Regarding using a plating process to form the gold grounding means, Wada et al. discloses a plating process to form gold contacts, therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose a plating process as disclose in Wada et al. in the primary reference of Lin et al. since plating processes are widely used in gild contact manufacturing processes.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Miyata discloses a process of singulating packaged semiconductor dies. Hively and Lin et al. discloses a method of preventing electrostatic discharge damage to a chip. Barrow discloses a method for making a ball grid array package referred in Lin et al..

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
November 18, 2004

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800